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TTL Tristate Hex Bus Drivers, 54365

G. T. Pham

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1.0 INTRODUCTION

The Generalized Emulation Microcircuit (GEM) program provides emulated integrated circuits (ICs) that are form, fit, and function equivalent devices for unavailable IC requirements. An emulated device meets all aspects of the original device's characteristics (e.g., the same physical dimensions, pin out, input/output (I/O) characteristics, and function). The GEM program is managed through Headquarters, Defense Logistics Agency as a part of their Manufacturing Science and Technology program. NRaD's Solid State Electronics Division has been involved in the program as Technical Direction Agent since its inception. NRaD also serves as the primary Design Technology Transfer site within the government. This document illustrates how to emulate the transistor-transistor logic (TTL) Tristate Hex Bus Driver (54365), with GEM technology.

2.0 OVERVIEW

The emulation of the TTL Tristate Outputs Hex Bus Drivers was completed in the GEM program. This device, which was emulated in a GEM gate array (Array384), combines MIL-M-38510/163A, Texas Instruments (TI), and Signetics data sheets. To design parts using GEM technology, custom I/O cells, both circuitry and layout are needed, because no standard I/O cells are available in the GEM design library. To complete this part, knowledge of analog design, spice simulation, logic simulation, and physical layout is required. These Tristate Outputs Hex Bus Drivers were emulated by using Bipolar Complementary Metal Oxide Semiconductor (BICMOS) technology and were fabricated at David Sarnoff Research Center (DSRC). The GEM BICMOS technology includes both bipolar transistors and 1.5-um CMOS transistors. The Array384, I/O, design approach, and the physical layout are discussed in later sections of this document.

3.0 DESIGN APPROACH

Not every part can be designed utilizing GEM technology. To make this determination, a few characteristics need to be examined, such as low-level input current (Iil), low-level output current (Iol), short-circuit output current (Ios), and the available gate arrays. If a part is "GEMmable," obtain the original part for testing purposes. Secondly, obtain the commercial and/or military data sheets for comparison purposes. Note that a military data sheet does not supply typical values; however, commercial data sheets commonly do. Testing or characterization of the original part is required for more accurate emulations. Maximum GEM capability to emulate a part per INPUT cell is Iil = –5 mA, and per OUTPUT cell is Iol = 20 mA, Ios = –55 mA. Iil, Iol, and Ios can be determined from the device's data sheet. If the part's values are greater than the individual cell capabilities, then two I/O cells are needed. The next step is to determine the proper gate array. The number of bond pads (for I/O cells) and core cells (for logic function) are two of the major criteria needed to ensure the array contains enough design elements.

From the MIL-M-38510/163A specification, the maximum Iil, Iol, Ios of TriState Outputs Hex Bus Drivers are –1.6 mA, 32 mA, and –130 mA respectively. Therefore, one input and two output cells will be used. The original part has 16 pins, including 6 inputs, 6 outputs, 2 control inputs, 1 power, and 1 ground. The GEM emulation will need 2 outputs cells per original output pin; the total bond pads should be equal to 22 pads (including the power and ground pads). Array384 will be used for this device.

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4.0 ARRAY384

Array384 was selected for this device because it provides adequate core space, pads, and die size. Array384 allows up to 28 bond pads, of which 26 are the I/O cells and two are dedicated to power and ground pads. This array includes 384 core cells. Each core cell contains four n-channel MOS (NMOS) transistors, four p-channel MOS (PMOS) transistors, three capacitors, and two resistors. The die size is approximately 2770 x 4484 μ. Figure 1 provides an overview of the base gate Array384 provided by DSRC.
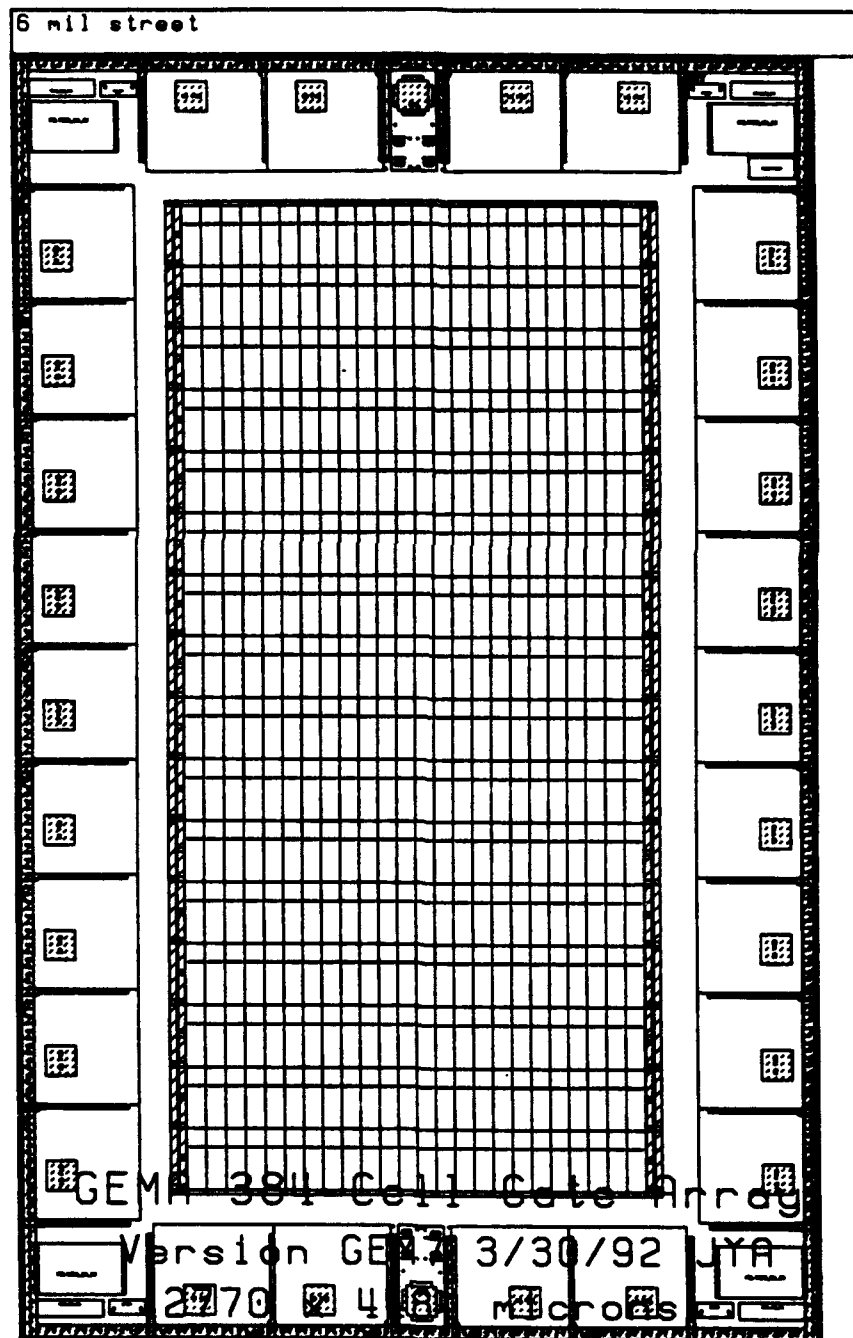

Figure 1. Array384

5.0 TRISTATE OUTPUTS HEX BUS DRIVERS

The schematic can be found on the commercial data sheet. The emulation of this device will be based on the TI schematic (figure 2).
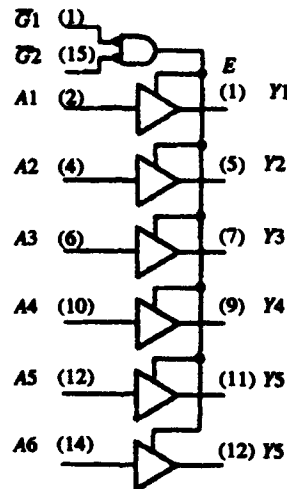
Figure 2. TI Tristate Outputs Hex Bus Drivers' schematic.

Usually, the necessary logic macro cells are contained in the standard cell library provided by DSRC. However, in this case, the tristate buffer in this design was not present. The tristate buffer is implemented by figure 3. Its functionality behaves no differently than other tristate buffers based on logic simulations. Note that figure 3 cannot be simulated by itself; it must be connected with an output cell to verify the functionality. In fact, a small disadvantage exists when using figure 3 for the tristate buffer. The implementation, which will take more core space, may be a major concern in a design. In this case, core space is not an issue. The following describes how the macro cell (figure 3) will fit into the TI Tristate Outputs Hex Bus Drivers' schematic (figure 2). The relationship is how the labels, DATA and ENABLE, of figure 3 correspond to the As and the enable pin (point E) of figure 2, respectively. However, INN1 and INN2 of figure 3 will connect to the two inputs of an output cell.
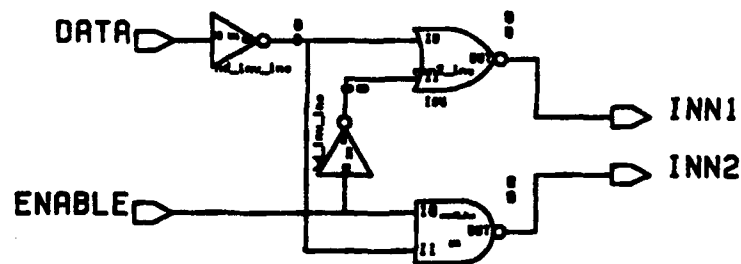
Figure 3. Tristate buffer core logic macros.

The core logic macros were already established, and their connection was just described. The final schematic and its truth table are presented in figure 4 and table 1, respectively. In figure 4, the two output cells are tied together due to a larger specification limit for Iol and Ios, as mentioned earlier in the design approach. Also, to reduce capacitance in the OUTPUT cell, a parallel pair of inverters are being implemented in the core section.

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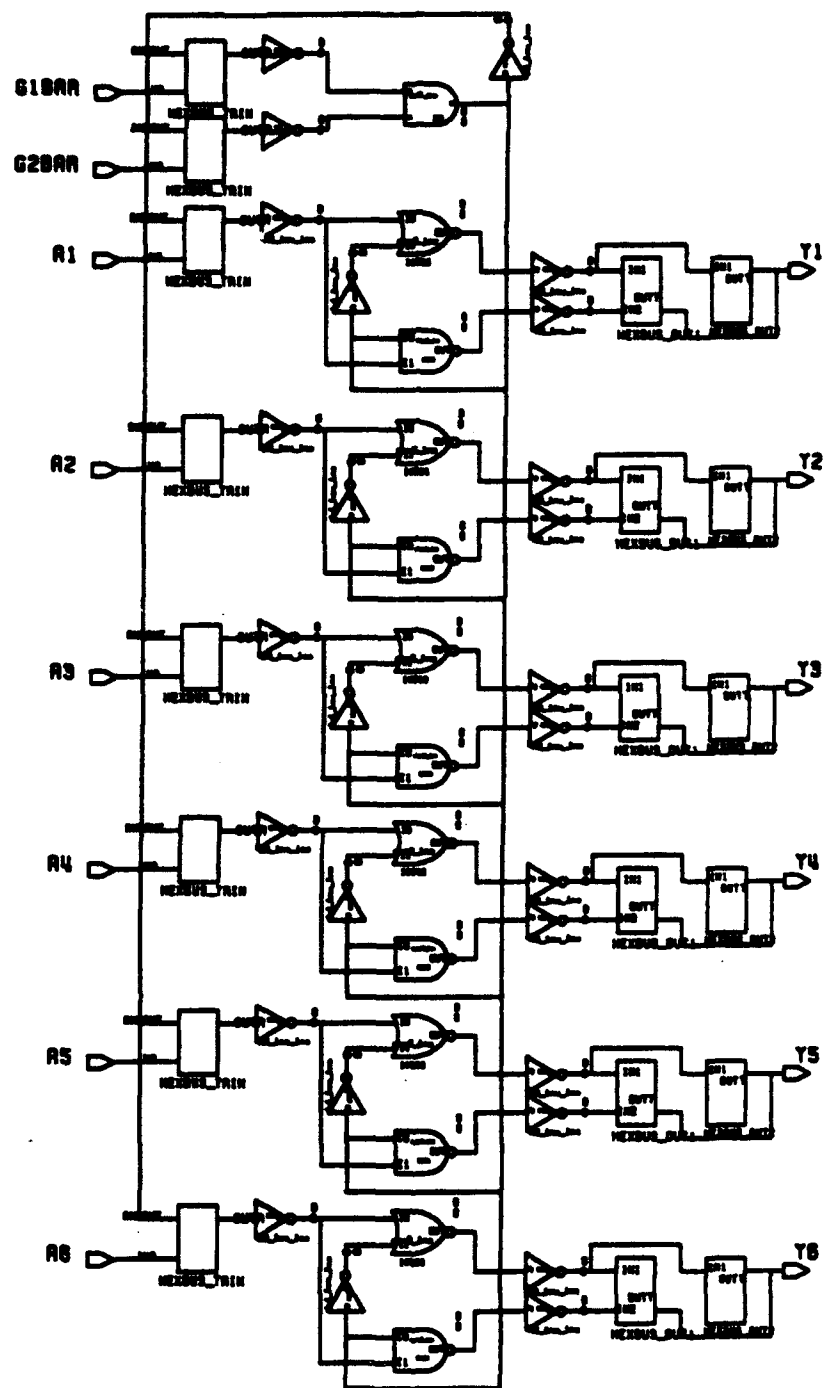
Figure 4. Final schematic of Tristate Outputs Hex Bus Drivers (with a special tristate buffer).

Table 1. Truth table of Tristate Outputs Hex Bus Drivers.

Inputs			Output
G1bar	G2bar	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

The function of each driver segment is described in table 1. G1bar and G2bar are two control inputs activated at low logic level. When either G1bar or G2bar is high, then the output Y will be a high-impedance Z regardless of the input. In the case when G1bar and G2bar are at low-logic level, they will activate, and output Y will follow input A.

6.0 I/O CELLS

The I/O cells serve as technology translators between the original part's technology and the CMOS core cells that perform the device's logic functions. These cells meet all DC/AC characteristics over the commercial or military temperature range.

6.1 INPUT CELL AND ITS SPICE SIMULATION

Since the core is straight CMOS technology, the input cell transfers from TTL voltage to CMOS voltage level. For an input cell design, Iil, Iih, Vth, voltage level shift, propagation delay, and Icc are the most important factors to be taken into consideration from the Spice simulations. The cell design must meet the specifications derived from the data sheet and the actual measurements.

Figure 5 represents the input circuit of the Tristate Outputs Hex Bus Drivers. The input cell is more complicated to design than is the output cell. The next paragraph briefly explains how the design is initiated. The PMOS MP5 device between the power supply and resistor R2 is needed to control the device for the tristate case. This PMOS MP5 (figure 5) is for toggling purposes. The current can flow from the Vdd power supply down when the MP5 is on.

When input is LOW (0.4 V), resistor (R2 + R2A) can be determined as the voltage drop between Vdd and V(IN) over current Iil where Vdd and Iil are 5.5 V and 1.257 mA respectively. Iil was determined from measuring the original part. Also V (diode) is approximately 0.7 V.

$$(R2 + R2A) = (Vdd - V(diode) - V(IN))/Iil. \tag{1}$$

For the case when input is high (2.0 V), (R3 | R3A) can be determined as the voltage drop between V(Q1 collector) and ground over the resistor (R3 | R3A). Equation (2) demonstrates the relationship. Also, VIN = V(Q1 collector).

$$(R3 | | R3A) = (V(IN) - 2*V(diode))/I, \tag{2}$$

where I is the current that flows from Vdd through (R2 + R2A), and it can be calculated as the voltage drop between Vdd and V(Q1 collector) over (R2 + R2A). Equation 3 will explain how it is determined.

$$I = (VDD - V(Q1 \; collector))/(R2 + R2A), \qquad (3)$$

where V(Q1 collector) = 2 V and (R2 + R2A) was previously determined.
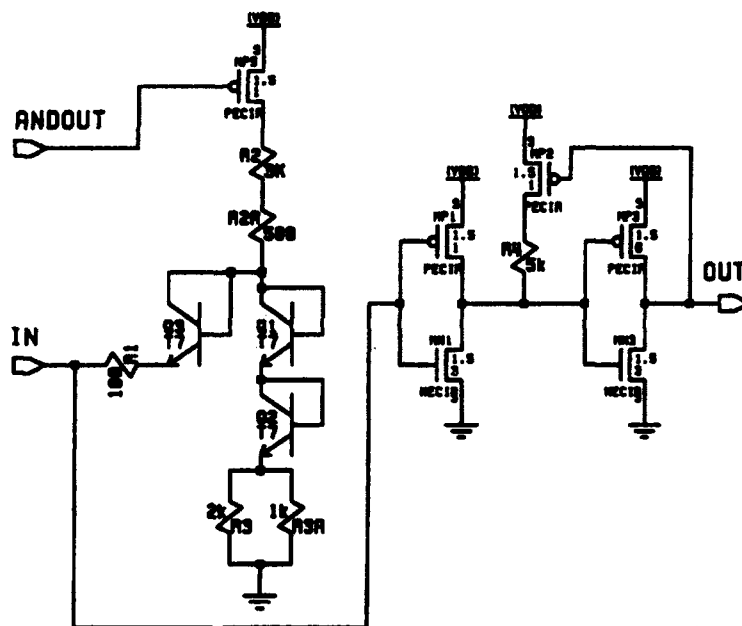
Figure 5. Input circuit of Tristate Outputs Hex Bus Drivers.

In any design process, simulation is a requirement to verify the accuracy of the design. Spice simulations are used to verify that the INPUT circuit is functional and meets the specifications such as Vth, Iil, and voltage translations. Figure 6 is the result of the spice simulation, indicating a threshold voltage at 1.5 V and Iil is approximately –1.2 mA. In comparison with the military data sheet, Vth and Iil are 1.5 V and –1.6 mA max, therefore these data simulations are acceptable. Also, the most significant factor is to make sure that Iil is totally shut off, or zero at 2 V and over. Figure 6 shows that Iil is completely shut off at 2 V and above, indicating no leakage current. Further confirmation is demonstrated with Iih equal to zero from Spice simulation.

The voltage level shift from TTL voltage level to CMOS voltage level demonstrates that the technology is transferable. Figure 7 shows the logic level shift from 3 V input to approximately 4.5 V output, rather than 5 V, because Vdd was forced to 4.5 V in the simulation to be consistent with the specification. Also, from figure 7, the propagation delay from the IN to OUT (figure 5) is within a few nanoseconds, as the graph display that tplh(IN →OUT) = 1.19 ns and Tphl(IN →OUT) = 1.7 ns. The propagation delay for the input cell is satisfactory.

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Figure 6. Spice simulation of Vth and Iil.

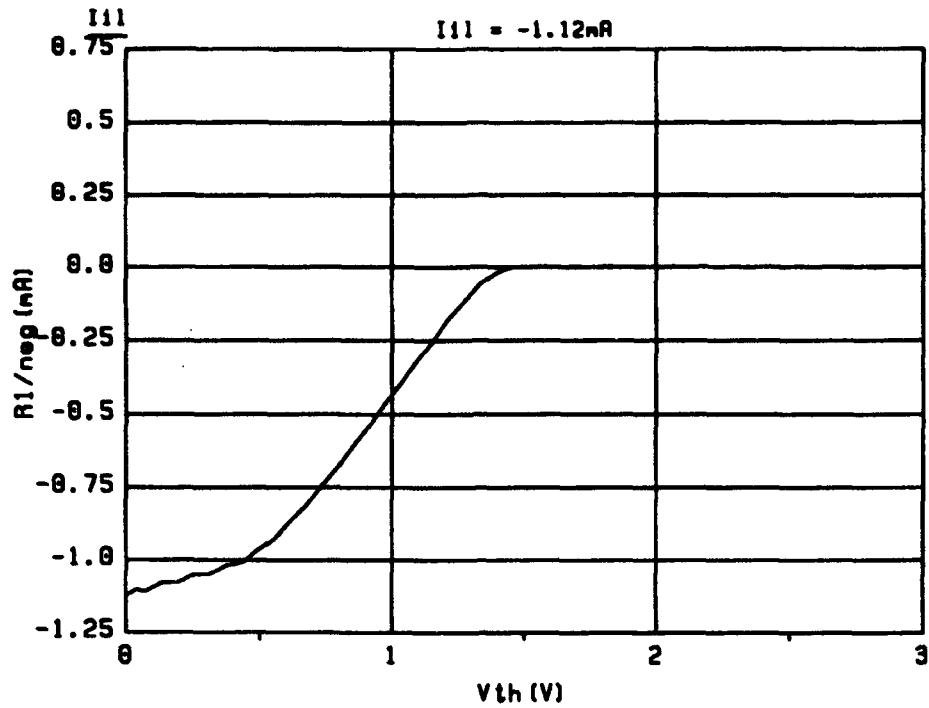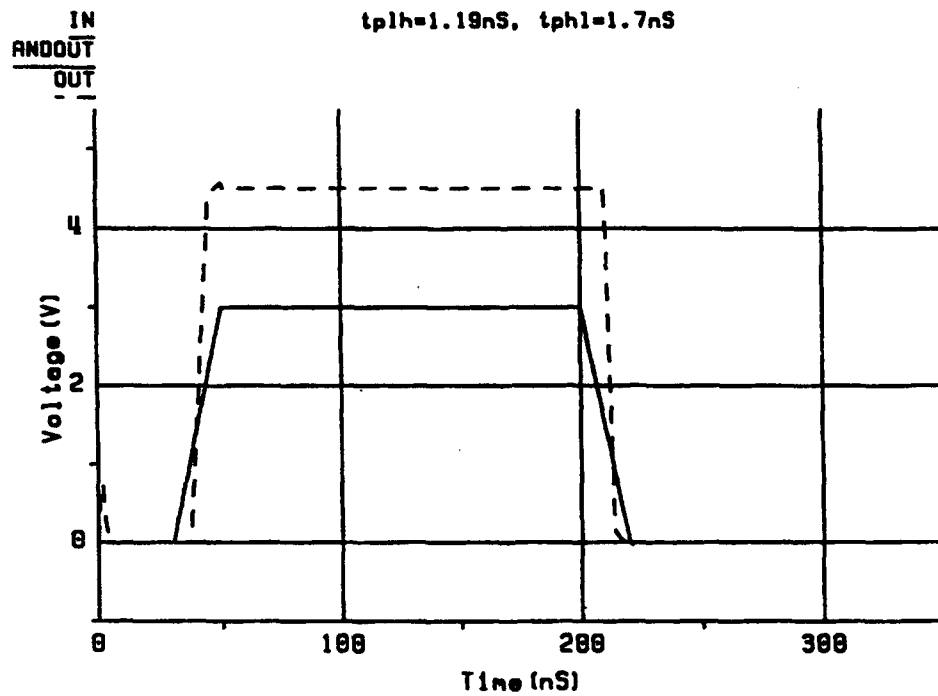Figure 7. Graph of the voltage shift and its propagation delay between IN and OUT of an input cell. (ref: Circuit in figure 5).

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The last major input design issue is the power supply current, Icc. Icc of input cell has been simulated and the result is displayed in figure 8 below, indicating that Icc per input (Icc/input) is approximately 1.13 mA. The Icc value listed in the data sheet is for the whole device. To achieve Icc for the entire design, the calculation is performed as in equation (4). By using equation (4), Icc(T) = 9.04 mA since 8 input cells are in this design, where Icc(T) is the total power supply current of the complete design/device. From military data, Icc(T) = 85 mA max. To compensate the difference between two values, additional resistors are needed to draw more current. In conclusion, this input cell design satisfactorily supports the Tristate Outputs Hex Bus Drivers based on the previous illustrations.

$$Icc(T) = (Icc/input) * \text{Number of inputs in the design} \qquad (4)$$
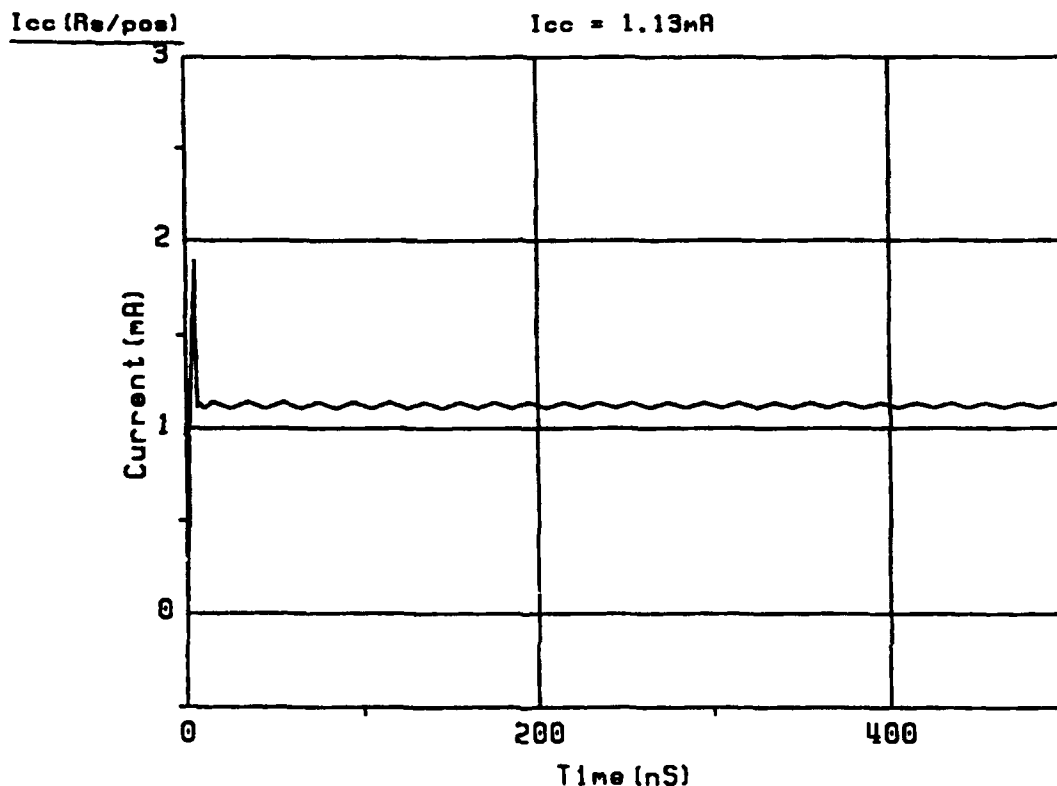
Figure 8. Graph of Icc per input cell.

6.2 OUTPUT CELL AND ITS SPICE SIMULATION

The output cell function is transferring from CMOS voltage level to the technology that is being emulated, in this case TTL. Technology transformation and matching is a primary purpose of emulation. The output circuit of the Tristate Outputs Hex Bus Drivers is displayed in figure 9. Figure 4 contains six instances of two paired output cells that have been broken apart in figure 9 for layout purposes. In other words, exploding to the next lower level of the two connected outputs in figure 4 is equivalent to the single circuit in figure 9. Output cell design is mostly based on the test measurement values of the original part. Its device sizes and other design factors will be discussed in a later section. Because the CMOS voltage level from the core enters output cells that are required to convert to TTL voltage level, some voltage drop is

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expected. In order to accomplish this, two level diodes connected in series are utilized for the voltage conversion (employing the voltage drop across the diodes).

The device size can be determined by using the test measurement of Ios, Vol, and Iol from the data sheet. Equation (5) is used to determine the total number of the PMOS device, P(tot dev).

$$P(tot\ dev) = 1/[(3.3\ mA/dev)(1/Ios)], \tag{5}$$

where 3.3 mA/device (a value from DSRC) is the amount of current per device from the measurement of the original part at 25 degrees Celsius.
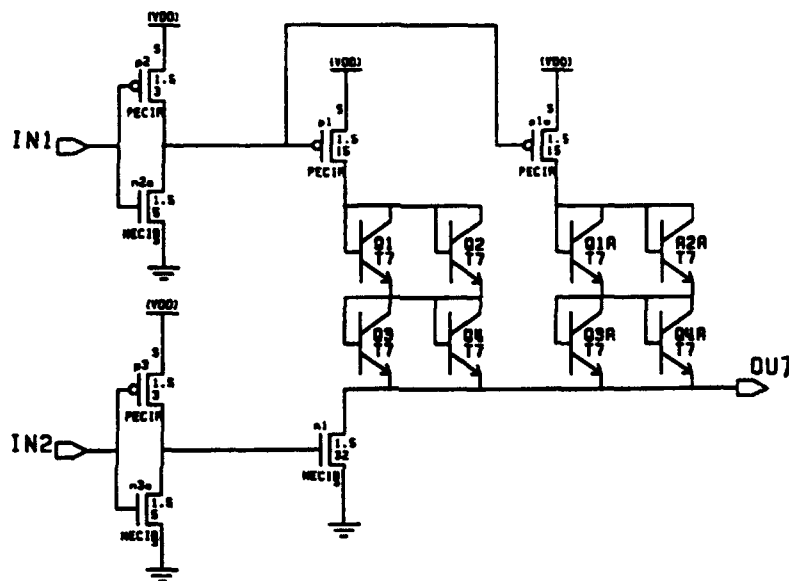
Figure 9. Output circuit of Tristate Outputs Hex Bus Drivers.

To calculate the total PMOS device size, only Ios is required. A value of Ios is –98 mA. When Ios is applied to equation (5), P(tol dev) is approximately 30 devices. These devices are broken up to be 15 on each side. The division and use of two parallel series is due to the physical limitations imposed by the current limitations.

Equation (6) is used to determine the total number of NMOS devices. With vol = 0.319 V and Iol = 32 mA, resistance can be calculated so the outcome of N(tol dev) is approximately 32 devices.

$$N(tot\ dev) = [n^2(315\ ohm/dev)(1/resistance)], \tag{6}$$

where resistance = vol/Iol in ohms and n is a single unit device. The value 315 ohms/dev is from DSRC.

In the output cell, voltage conversion is a major issue. Additional important concerns are the AC characteristics such as tplh (propagation delay from low to high), tphl (propagation delay from high to low), tr (rise time), and tf (fall time). They should be checked to make sure they meet the specifications. In this design, those characteristics have been checked and the results from simulation are shown in figure 10. The values on top of the graph indicate the propagation delay, rise and fall time of the output cell. The delays are within the specification range. Therefore, the output cell is adequate for the design.

Figure 10. Output cell simulation for voltage transfer, delay, and rise and fall time.

7.0 SIMULATIONS

7.1 LOGIC SIMULATION

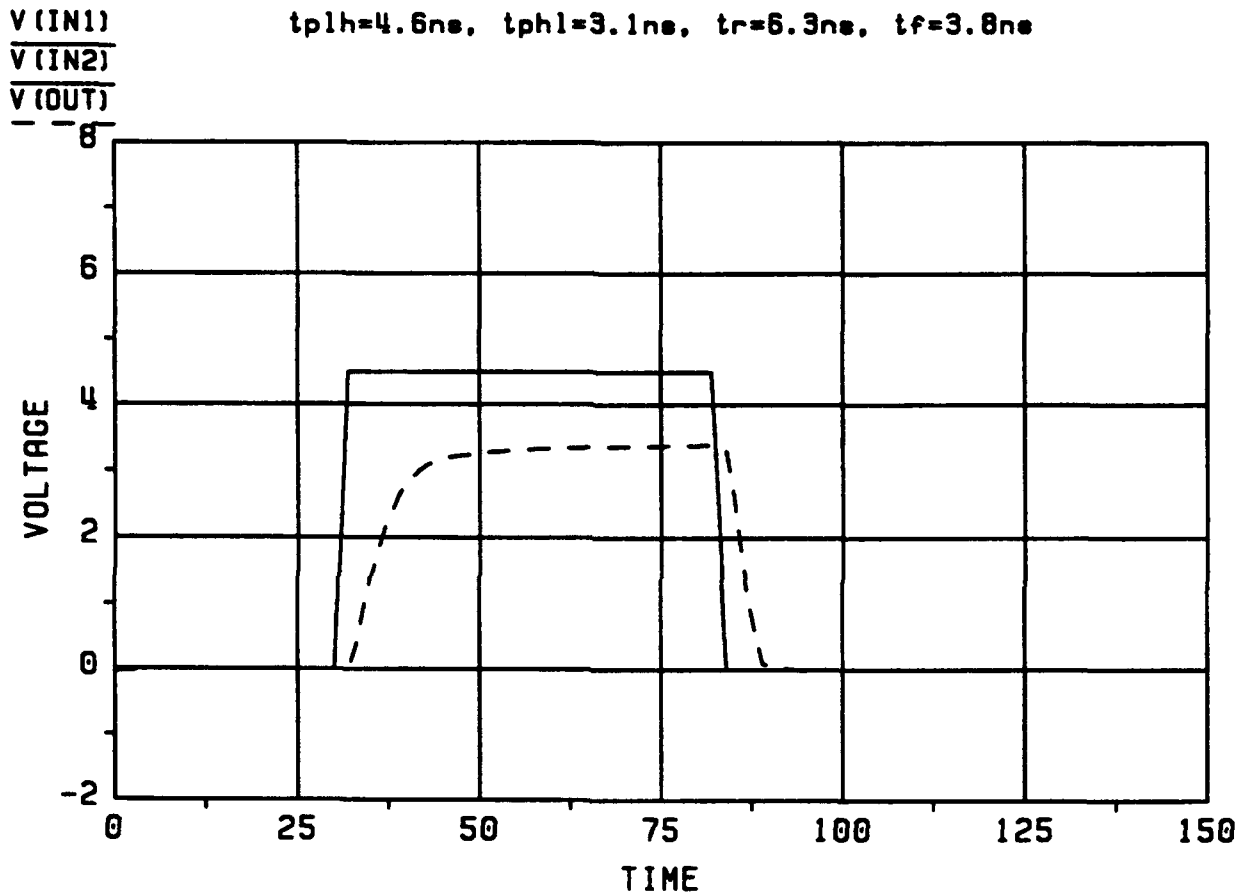One critical design/emulation requirement is to meet all specifications. Full functionality is another important factor. Logic simulation is performed to verify the functionality of the Tristate Outputs Hex Bus Drivers' design. Below (figure 11) is the output logic simulation displayed in both waveform and binary formats; both outputs describe the same function. For a better visualization, only two drivers are shown. The rest of the drivers are essentially the same.

Based on the simulation, if either of the control inputs, G1bar or G2bar, are HIGH, the device is disabled, or in a high-impedance state. Both of the control inputs G1bar and G2bar must be a logic LOW to activate the device, the output Ys will then follow the input As. The states 1Z and 0Z in the binary table (figure 11) are in high-impedance states. For the cases when 1Z and 0Z occur (e.g., on the Nth clock cycle), the device is not enabled and the output of the previous (N-1) clock cycle was either 1 or 0, then the output at the N clock cycle will carry the N-1 Boolean value with an high-impedance state. In other words, 1Z and 0Z occur depending on the previous output state. The simulations prove that the device is functional based on its output and truth table indications.

7.2 SPICE SIMULATION

For emulated parts, all data should meet specifications at room temperature 25, and at military temperature ranging from -55 to 125 degrees Celsius and be compared with the military data sheet. On this device, all the simulations were completed only at 25 degrees Celsius per the contractor recommendations. The rational was that the models were designed and most accurate at 25 degrees Celsius. Thus, the decision was made that military temperature simulation be omitted until newer models are available.

7.2.1 DC Characteristics

Summary DC characteristics of the Spice simulation and military test data are shown in table 2. One representative driver segment (A1) is listed on the table. The table contains the test/simulation conditions and their associated results. The adjacent columns "Simulation Value" and "Military Test Value" may be compared and one can conclude that these simulation values are within specification.

7.2.2 AC Characteristics

In any emulation design, propagation delay is always involved. The propagation delay of the whole design was simulated by driving a TTL load to ensure that the specifications are met. The load is specified by the Signetics data sheet. MIL-M-38510/163A provides insufficient data about AC characteristics for simulation. The Signetics data sheet provides clear and direct data regarding AC characteristics. Figure 12 shows the TTL load that was used in this design for simulation purposes (and may be used for testing). S1 and S2 are two switches that toggle for the tristate purpose. Vdd is 5 V and RX, and RL are 1000 ohms and 400 ohms respectively. Load capacitor (CL) is given depending on the states. Pin Y connects to the output of the drivers. Refer to table 3 for additional data values.
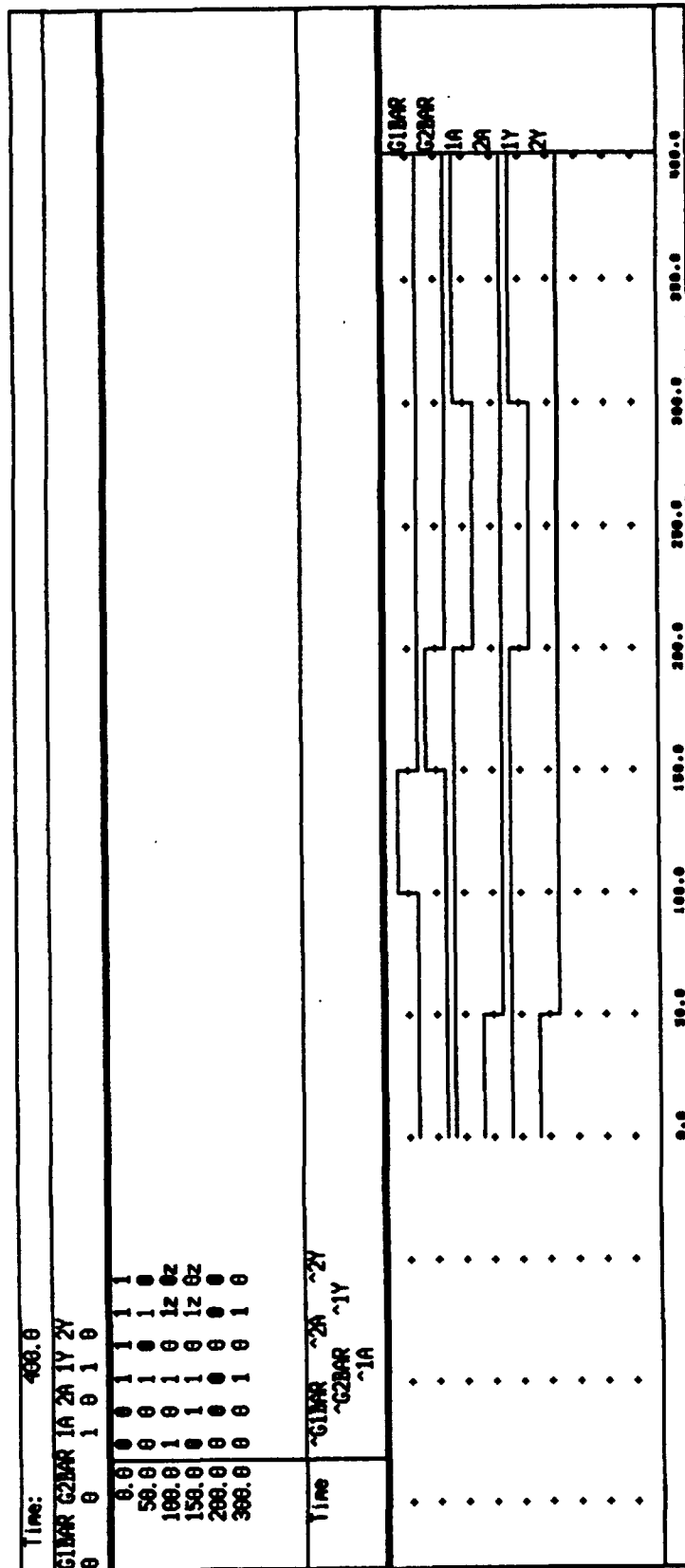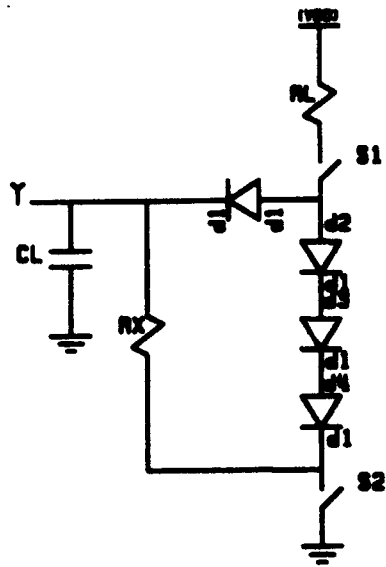
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Figure 11. Output of logic simulation of 54365 design.

Figure 12. TTL load of 54365 design.

Table 2. DC characteristics of spice simulation and military test value.

Symbol	G1bar	G2bar	A1	Y1	Vdd	Measured Terminal	Military Test Value		Simulation Value	Unit
							Min	Max		
Voh	V, 0.8	V, 0.8	V, 0.8	mA, -2.0	V, 4.5	Y1	2.4		3	V
Vol	V, 0.8	V, 0.8	V, 0.8	mA, 32.0	V, 4.5	Y1		0.4	0	V
Io1	V, 2.0	V, 0.8	V, 0.8	V, 2.4	V, 5.5	Y1		40	0	uA
	V, 0.8	V, 2.0	V, 2.0	V, 2.4	V, 5.5	Y1		40	0	uA
Io2	V, 2.0	V, 0.8	V, 0.8	V, 0.4	V, 5.5	Y1		-40	0	uA
	V, 0.8	V, 2.0	V, 2.0	V, 0.4	V, 5.5	Y1		-40	0	uA
Iih1	V, 2.4				V, 5.5	G1bar		40	0	uA
		V, 2.4			V, 5.5	G2bar		40	0	uA
			V, 2.4		V, 5.5	A1		40	0	uA
Iih2	V, 5.5				V, 5.5	G1bar		1	0	mA
		V, 5.5			V, 5.5	G2bar		1	0	mA
			V, 5.5	V, 5.5	V, 5.5	A1		1	0	mA
Iil1	V, 2.0	V, 2.0	V, 0.5	V, 0.5	V, 5.5	A1		-40	0	uA
Iil2	V, 0.4	V, 0.4	V, 0.4	V, 0.4	V, 5.5	A1		-1.6	-1.12	mA
Iil3	V, 0.4				V, 5.5	G1bar		-1.6	-1.02	mA
					V, 5.5	G2bar		-1.6	-1.02	mA
Ios	V, 0.8	V, 0.8	V, 0.8	V, 5.5	V, 5.5	Y1	-40	-130	-54.5	mA
Icc	Gnd	Gnd	Gnd	Gnd	V, 5.5	Vdd		85	9.04	mA

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Table 3. AC characteristics.

Symbol	G1bar	G2bar	A1	Y1	Vdd	Measured Terminal	Military Test Value		Simulation Value	Unit
							Min	Max		
Tplh	Gnd	Gnd	Gnd	A, *	Out	V, 5.0	2	16	6.1	ns
Tphl	Gnd	Gnd	Gnd	A, *	Out	V, 5.0	2	22	5.4	ns
Tpzh	B, *	Gnd	Gnd	V, 2.0	Out	V, 5.0	G1bar to Y1	2	35	10.57	ns
Tpzl	Gnd	C, *	Gnd	V, 0.8	Out	V, 5.0	G2bar to Y1	2	37	9	ns
Tphz	D, *	Gnd	Gnd	V, 2.0	Out	V, 5.0	G1bar to Y1	2	16	10.05	ns
Tplz	E, *	Gnd	Gnd	V, 0.8	Out	V, 5.0	G1bar to Y1	2	27	6.88	ns

(For the first two rows, Measured Terminal = A1 to Y1.)

	S1	S2	CL	RL	RX	Vdd
A	Closed	Closed	pF, 50	Ohm, 400	Ohm, 1000	V, 5
B	Open	Closed	pF, 50	Ohm, 400	Ohm, 1000	V, 5
C	Closed	Open	pF, 50	Ohm, 400	Ohm, 1000	V, 5
D	Closed	Closed	pF, 5	Ohm, 400	Ohm, 1000	V, 5
E	Closed	Closed	pF, 5	Ohm, 400	Ohm, 1000	V, 5

* = Force a signal

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8.0 I/O CELLS LAYOUT

Since the I/O cell is custom designed for each device, I/O cell layout is required to complete the physical design. The base I/O cell is provided by DSRC as displayed in figure 13. The base I/O cell contains predefined PMOS transistors, NMOS transistors, Bipolar transistors, and resistors. The PMOS and NMOS transistors are designed in a circular architecture with the length equal to 1.5 um. Briefly, sections 1, 2, 3, and 4 of figure 13 are PMOS, NMOS, Bipolar transistor, and resistor tank respectively.
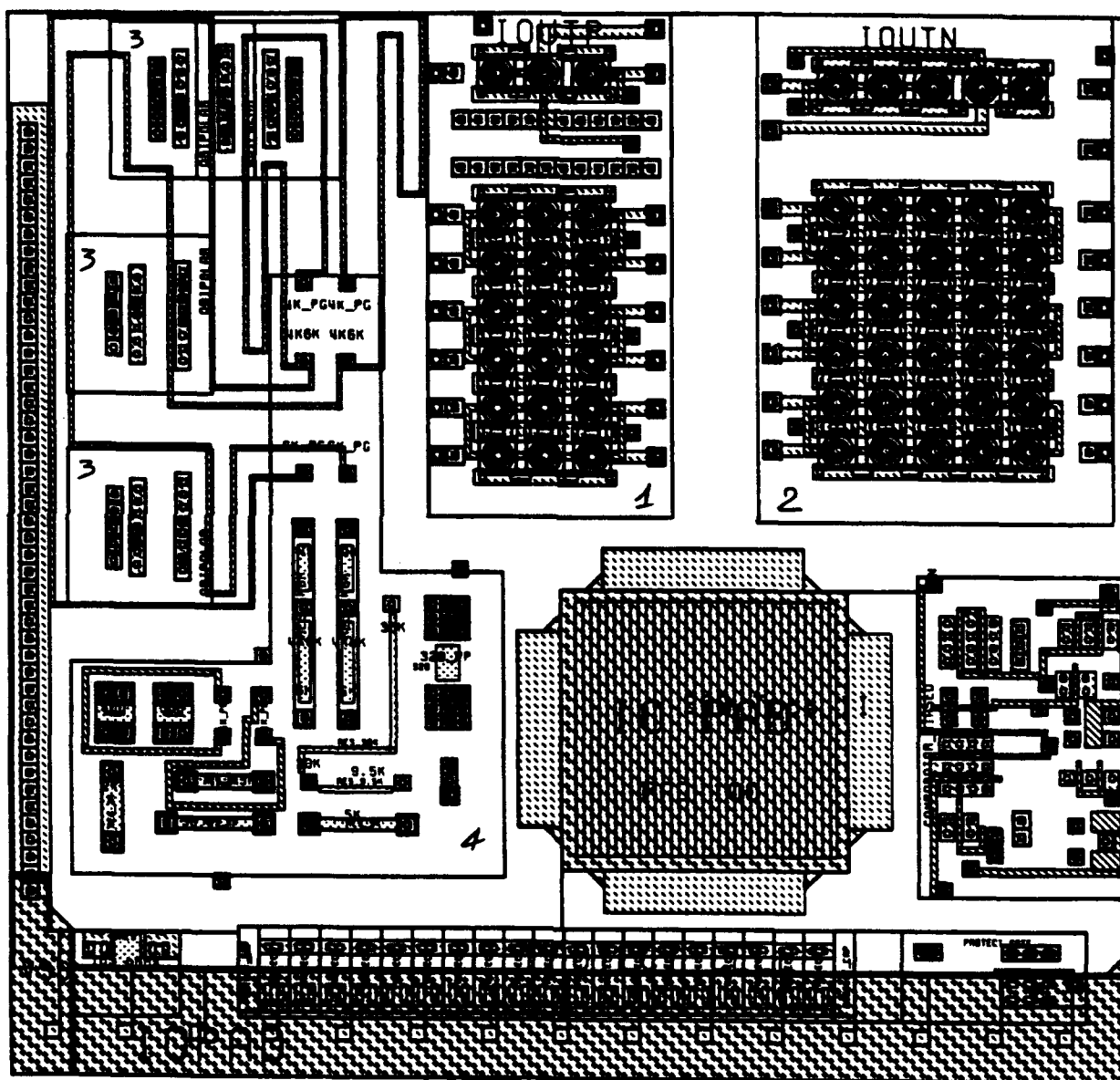
Figure 13. Base I/O cell.

The above I/O cell can be wired into either an INPUT or OUTPUT configuration corresponding to the schematic. When the I/O cell is designed as an input, the I/O cell translates the input technology to the CMOS core technology. The base I/O cell by itself is not functional until it is all wired as either an INPUT or OUTPUT. Figure 14 is an INPUT cell after it is wired

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together. The metal lines connect the MOS and bipolar transistors, and protection devices corresponding to the required designed circuitry. The designer must follow the design rules during the physical layout phase of the I/O cell.
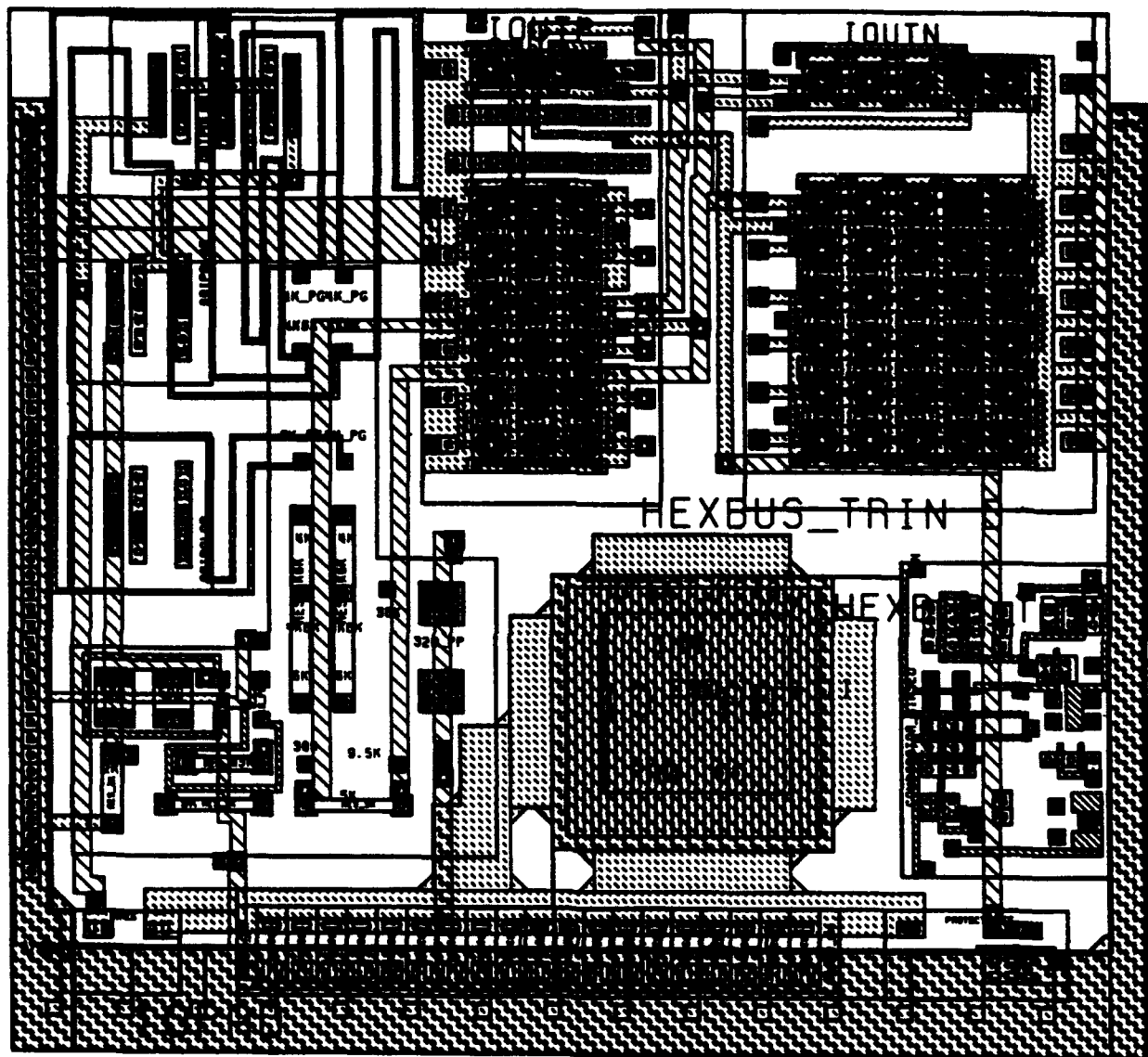

Figure 14. Input cell layout of 54365.

The OUTPUT cell translates from a CMOS level to a TTL voltage level. Because of the large number of the devices used in the design, two I/O cells are required to complete the layout. The procedures for completing the OUTPUT cell layout are similar to the INPUT except that two I/O cells must be interconnected to make a complete OUTPUT layout that satisfies the design requirement. The interconnection (two I/O cells) must be performed manually, presenting a greater challenge than the INPUT cell. The metal running on top of figure 15 is the connection from one I/O cell to the other. The final OUTPUT layout is shown in figure 15.
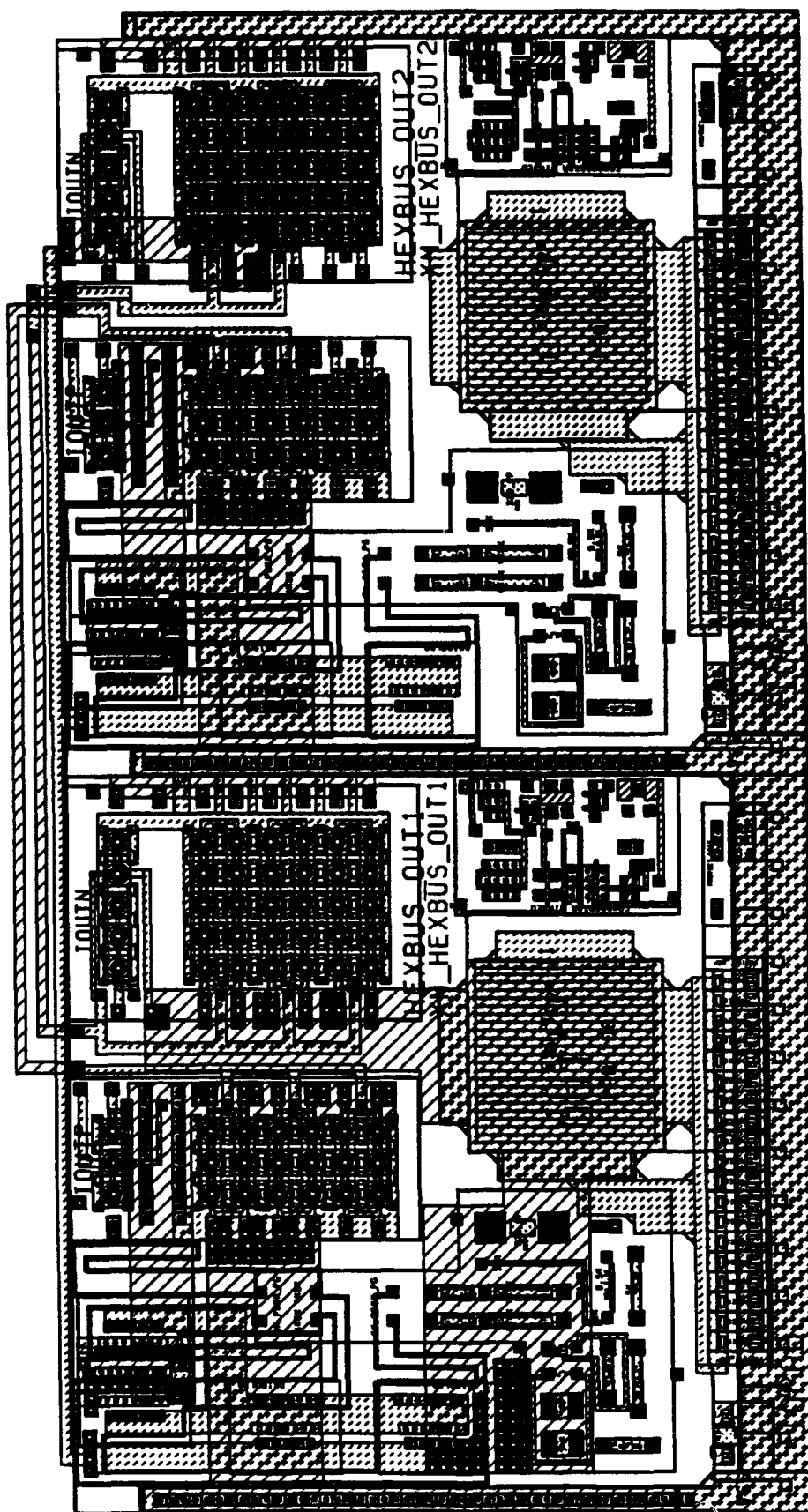
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Figure 15. Two I/O cells are used for the OUTPUT.

The next step, combining the I/O layout with logic cell layout and with the gate array, uses Gatestation to perform the physical layout design. The logic cell and gate array elements are from the library, but the I/O cells were custom layouts by the designer.

9.0 PHYSICAL LAYOUT DESIGN

The physical layout design was completed mainly using Gatestation and Chipgraph tools. The following are the individual commands to perform the physical layout design. Each of the commands should be of the form design_name, tech_name, and array_name unless otherwise specified.

Usage:
gem_expand_comp < design_name> <tech_name> <array_name>
gem_expand_design
gem_pkg_def <design_name> <tech_name> <array_name> <pack_name>
gem_layout logic_entry
gem_layout gateplace
gem_layout gateroute
gem_layout pregraph
gem_layout gategraph

Note: tech_name = bicmos1
        pkg_def = package definition

The expand command creates a flattened design database. The pkg_def command creates the pin out diagram, and the designer may determine how to place the pins. Logic entry is the first stage of physical layout design and its purpose is to create the physical design file from the logic design file. Gateplace and Gateroute perform automatic placing and routing/connection. Pregraph and Gategraph bring the graphic design into Gatestation after placement and route. For an optimum way to perform the physical layout, it is best to create a batch file containing these commands and run them all at once.

After completion of place and route, Gatestation will automatically invoke with the design. From this point, the design can be saved and one should exit Gatestation. The next step is to convert Gatestation output into a Chipgraph database using the command below. A separate directory must be employed to perform this function.

Usage:
chipgraph_output <design_name> </user/gem/bicmos1/arrayXXX> -c
</user/gem/bicmos1/cdb_outfile>

Note:
arrayXXX = array_name

In this case, Array384 was used for the design. Therefore, the correct nomenclature should be Array384 instead of arrayXXX. The following summary procedure describes how the design is converted into a Chipgraph database. Invoke Chipgraph and read in the process file by clicking on the menu button. The design is brought in, instantiates the gate array, frame, and text, and yields a complete design. Below are the detailed procedures.

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1. Invoke Chipgraph and edit the Gatestation's Chipgraph cell; call it "design." Load in the process first.

2. Activate Array_384 and instantiate it at the origin of "Design."

3. Add a perimeter (silhouette, add per boundary). Delete array_384.

4. Save and exit the window for "Design."

5. Edit cell called "Array_design."

6. Activate and instantiate all the following cells at the origin:

    a.   Array_384
    b.   "Design"
    c.   Array_384_vssvdd
    d.   Array_384_bus

7. Now select all the cells and peek (a command) just 1 level down.

8. Add M1 for Vss and M2 for Vdd at the point that Vss and Vdd are used.

9. Add a shape of metal 1 to the pads and add the port names to each block for LVS purposes.

10. It is now ready to run DRC and LVS.

The complete gate array is shown in figure 16.

The next step is performing Design Rule Check (DRC) and Layout Versus Schematic (LVS). The purpose of running DRC and LVS is to make sure design rules and circuitry are matched with the layout before a design is sent out for fabrication. Conventional DRC and LVS of the I/O cell itself should be done before proceeding with the physical layout design. DRC and LVS command files are available in the system. Both DRC and LVS were performed and all of their flagged errors were resolved.

10.0 CONCLUSION

This paper was written to help new designers with future emulation of the project. It was also written as documentation of GEM design technology transferability. Detailed physical techniques for emulating a part are not available anywhere in our library. The above physical layout tools are brought into the discussion because the author believes that this is very valuable information. The GEM design manual does not describe complete information on how to perform physical layout design. This paper was written with an assumption that designers are familiar with the design tools such as Neted, Quicksim, Mspice, Gatestation, Chipgraph, and Dracula. The design of the 54365 (Tristate Output Hex Bus Drivers) is successfully completed, fabricated, and tested.

Figure 16. Complete gate array of the Tristate Output Hex Bus Drivers.

11.0 GLOSSARY

BICMOS   Bipolar Complementary Metal Oxide Semiconductor

CL   Load capacitor

CMOS   Complementary Metal Oxide Semiconductor

DRC   Design Rule Check

DSRC   David Sarnoff Research Center

GEM   Generalized Emulation Microcircuit

IC   Integrated circuit

I/O   Input/Output

LVS   Layout Versus Schematic

MOS   Metal Oxide Semiconductor

NMOS   n-channel MOS transistor

PMOS   p-channel MOS transistor

TI   Texas Instruments

TTL   Transistor-transistor logic

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This report details the emulation of the TTL Tristate Outputs Hex Bus Drivers, which was completed in the GEM program. This device, emulated in a GEM gate array (Array384), combines MIL-M-38510/163A, Texas Instruments (TI), and Signetics data sheets.

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